REMARKS

Rejection Under 35 USC §112

Claim 25 has been rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter. This rejection is based on the term "chip scale" in claim 25, line 3. In response to this rejection, claim 25 has been amended to remove the "chip scale" limitation.

Rejections Under 35 USC §103

Claims 25-37, 29-33, 35, 36, 38, 39 and 47-53 have been rejected under 35 USC 103(a) as being unpatentable over Chou et al. (US Patent No. 5,691,568) in view of Liu et al. (US Patent No. 5,693,568).

Claim 28 has been rejected under 35 USC 103(a) as being unpatentable over Chou et al. (US Patent No. 5,691,568) and Liu et al. (US Patent No. 5,693,568) and further in view of Hembree (US Patent no. 5,783,461).

Claims 34 and 37 have been rejected under 35 USC 103(a) as being unpatentable over Chou et al. (IUS Patent No. 5,691,568) and Liu et al. (US Patent No. 5,693,568) and further in view of Pedder (US Patent No. 5,717,245).

The rejections under 35 USC §103 are traversed for the reasons to follow.

Summary of the Invention

Claims 25-39 and 47-53 are directed to a "semiconductor component". The component includes a substrate 10 (Figure 2), and a conductive layer 14 (Figure 2) substantially covering the substrate 10. In addition, the component includes conductors 16 (Figure 2) defined by

grooves 15 (Figure 2) in the conductive layer 14 (Figure 2), and a semiconductor die 20 (Figure 2E) on the conductive layer 14 (Figure 2E) in electrical communication with the conductors 16. As shown in Figure 2C, the conductors 16 comprise portions of the conductive layer 14 separated by the grooves 15, and by remaining portions of the conductive layer 14 having edges defined by the grooves 15.

35 USC §103(a) Rejections Of Claims 25-37, 29-33, 35, 36, 38, 39 and 47-53 Over Chou et al. and Liu et al.

Independent claims 25, 30, 35, 47 and 52 have been amended to emphasize the features that make the claimed component unobvious over the prior art. Specifically, in the claimed component the conductive layer 14 (Figure 2B) "substantially covers" the substrate 10 (Figure 2B). As shown in Figures 2-2E, the only portions of the substrate 10 not covered by the conductive layer 14 are the portions that align with the micron sized grooves 15 (Figure 2D). In addition, as shown in Figure 2E, the die 20 (Figure 2B) is mounted "on" the conductive layer 14 (Figure 2B).

One advantage of the claimed construction, is that the conductive layer 14 provides rigidity and heat transfer for the substrate 10. In addition, the die 20 is in direct thermal communication with the conductive layer 14. Further, the grooves 15 (Figure 2D) define and provide electrical isolation for the conductors 16 (Figure 2), while the conductive layer 14 (Figure 2B) remains intact. Still further, the grooves 15 (Figure 2D) can be made very small and accurately shaped using a laser machining process.

Figures 10A and 10B of Chou et al. were cited as disclosing a substrate having a conductive layer (512, 1011a-d) which forms conductors. However, as shown in Figure 10B, only a small percentage of the substrate (i.e., less than half) is covered by the conductive layer (512, 1011a-d). In addition, as shown in both Figures 10A and 10B, the die 502 is mounted on the substrate, rather than on the conductive layer (512, 1011a-d).

Figures 11A and 11B of Chou et al. were cited as teaching an electrically conductive die attach area 1180 (Figure 11A) for the die 502 (Figure 11B). However, the Examiner has combined two different embodiments of Chou et al. (Figures 10A and 10B with Figures 11A and 11B) but with no motivation for the proposed combination. Further, as shown in Figure 11A Chou et al., the conductive layer (1180, 511a-d), still covers only a small portion of the substrate (i.e., less than half). Admittedly, metal die attach areas are known in the art. However, in the present component, the die is mounted to a conductive layer that covers the substrate, except for the portions aligned with the micron sized grooves.

In addition to the "substantially covers", and the die "on" the conductive layer limitations, independent claim 30 and 47 also state that the die is "flip chip" mounted to the conductive layer. Antecedent basis for this recitation is contained on page 14, line 24 of the specification. The prior art does not disclose or suggest a conductive layer which substantially covers a substrate, and provides conductors configured for flip chip mounting for a die. Although the prior art discloses flip chip mounting structures, the configuration of the present conductive

layer and conductors is submitted to be novel and unobvious over this art.

Another feature of the present component not disclosed or suggested by the art is that the grooves have a "same micron sized width". This feature is recited in independent claims 35, 47 and 52. Liu et al. was cited as teaching "conductor/interconnect pattern having feature size/width and spacing being 0.3-0.4 microns or greater". However, there is no suggestion in Liu et al. of forming micron sized grooves of equal width in a conductive layer which substantially covers a substrate.

The Office Action further states that "the width of each groove/conductor being equal to about 5 microns as taught by the embodiment of Fig. 11A/11B in Chou et al. and Liu et al.". However, Applicant is unable to locate any teaching in Chou et al. of equal width grooves between elements 1180 and 511a-d in Figure 11A. Rather, the grooves between elements 1180 and 511a-d are unequal. For example, elements 534c and 534d in Figure 11A of Chou et al. are separated by one eight of an inch, whereas elements 511d and 511b are separated by one sixteenth of an inch. In Figure 10A of Chou et al., elements 1011d and 1011c are separated by less than one sixteenth of an inch, whereas elements 1011c and 512 are separated by more than one sixteenth of an inch. Applicant thus submits that Chou et al. "teaches away" from the formation of equal sized grooves. As held in US v. Adams, 383 US 39, 148 USPQ 479 (1966), one indicium of unboviousness is "teaching away" from the claimed invention by the prior art.

Liu et al. teaches features having a 0.3-0.4 micron scale. However, Applicant is unable to locate any teaching in Liu et al. of a substrate substantially covered by a

conductive layer having micron sized grooves of an equal width.

The Office Action further states the "determination of parameters such as conductor dimensions . . . . . is a subject of routine experimentation". However, as exemplified by the method claims in issued parent case US Patent No. 6,107,119, the formation of the conductive layer with micron sized grooves involved more than routine experimentation. Also, the prior art does not disclose a substrate covered by a conductive layer with micron sized grooves of equal width, so there would be no equivalent structure on which to perform routine experimentation.

Another distinguishing feature of the present component recited in claims 29, 38 and 50 is that "the conductive layer and the width are selected to facilitate laser machining of the grooves". The Examiner has characterized these claims as "product by process" claims. However, a product produced by a laser machining process is not being claimed. Rather, specific elements of the component (i.e., the conductive layer and the width) are being described in the context of their suitability for laser machining. If an element of a product is configured for fabrication by a certain process, this is a feature of the element, regardless of what process is used to fabricate the product. For example, "KOOL AID" includes elements configured for dissolving in water. If a claim specifies an element of "KOOL AID" is configured to dissolve in water, this is a feature of the element, regardless of the process by which the "KOOL AID" is made.

35 USC §103(a) Rejections Of Claims 28 Over Chou et al. and Liu et al and Hembree et al.

Hembree et al. was cited as teaching a package having a semiconductor die flip chip bonded to pads on conductors. As previously argued, flip chip bonding structures are known in the art. However, the present flip chip bonding structure includes a conductive layer substantially covering a substrate having grooves and conductors. The claimed flip chip bonding structure is submitted to be novel and unobvious over the art.

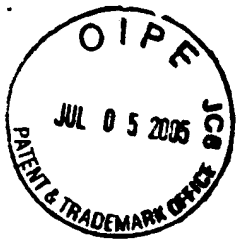
35 USC §103(a) Rejections Of Claims 34 and 37 Over Chou et al. and Liu et al and Pedder

Pedder was cited as teaching an encapsulant covering a die and a surface of the substrate. Admittedly, encapsulants are well known in the art. However, claims 34 and 37 have been amended to recite the encapsulant in combination with the conductive layer, the conductors and the grooves. As previously argued, the presently claimed conductive layer, conductors and grooves have a unique structure and function. Accordingly, claims 34 and 37 are submitted to be unobvious over the prior art.

Conclusion

In addition to the amendments to the claims, the title has been amended to be more descriptive of the claimed subject matter.

In view of the amendments and arguments, favorable consideration and allowance of claims 25-39 and 47-53 is requested. Should any issues remain, the Examiner is asked to contact the undersigned by telephone.



DATED this 29th day of June, 2005.

Respectfully submitted:

Stephen A. Gratton
Registration No. 28,418
Attorney for Applicant

2764 South Braun Way
Lakewood, CO 80228
Telephone: (303) 989 6353
Fax: (303) 989 6538

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class mail in an envelope addressed to: Mail Stop RCE, Commissioner For Patents, PO BOX 1450, Alexandria VA 22313-1450 on this 29th day of June, 2005.

June 29, 2005
Date of Signature

Stephen A. Gratton, Attorney for Applicant